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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/629,708	07/30/2003	Hidemitsu Mori	Q76698	5360

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SUGHRUE MION, PLLC
2100 PENNSYLVANIA AVENUE, N.W.
SUITE 800
WASHINGTON, DC 20037

EXAMINER	
CAO, PHAT X	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 05/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/629,708	MORI, HIDEMITSU	
	Examiner	Art Unit	
	Phat X. Cao	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-13 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-13 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 7/30/03.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kazushi (JP. 11-317500 – cited in IDS) in view of Lee et al (US. 5,895,947).

Regarding claims 1, 5-6 and 10, Kazushi (Figs. 2 and 8) discloses a semiconductor memory device, comprising: a semiconductor substrate 1; a memory cell section (Fig. 2) including a memory cell transistor 3 formed on the semiconductor substrate 1; a plate contact section (Fig. 8) including a plate transistor 4 formed on the semiconductor substrate 1; a first interlayer insulation film 11 formed on the semiconductor substrate 1 to cover the memory cell transistor 3 and the plate transistor 4; a ferro-electric capacitor 30 (Fig. 2) including a lower electrode 13 connected to the memory cell transistor 3, a ferro-electric film 14 (par. [0132]) and an upper electrode 15 and formed on the first interlayer insulation film 11 in the memory cell section; a second interlayer insulation film 16 being planarized and formed on an entire surface of the substrate to cover the ferro-electric capacitor; a first contact hole 17 (Fig. 2)

corresponding to the ferro-electric capacitor and formed in the second interlayer insulation film 16 in the memory cell section to expose the upper electrode 15 of the ferro-electric capacitor; a second contact hole 19 (Fig. 8) formed in the second interlayer insulation film 16 in the plate contact section; contact studs 18 formed in the first and second contact holes; and a plate line 18 provided to connect the upper electrode 15 and the plate transistor through the first contact hole 17 and the second contact hole 19 (see translation, par. [0145]).

Kazushi does not disclose an etch stop layer formed on the first interlayer insulation film 11 (claim 1) and made of a material which is different from the material of the first interlayer insulation film 11 (claim 10).

However, Lee (Fig. 8) teaches the forming of a first interlayer insulation film 130 formed on a semiconductor substrate 100 to cover a memory cell transistor and a plate transistor, and the forming of an etch stop layer 134 (column 3, lines 19-27) on the first interlayer insulation film 130 and made of SiN which is different from SiO of the first interlayer insulation film 130 (column 5, lines 1-11). Accordingly, it would have been obvious to modify the device structure of Kazushi by forming the etch stop layer on the first interlayer insulation film 11, and between the first interlayer insulation film 11 and the second interlayer insulation film 16 because such etch stop layer is well known and commonly used in the art for preventing the over-etching of the conductive layer to the underlying layer.

Regarding claim 2, Lee (Fig. 8) further teaches: a first conductor e1 formed to penetrate the first interlayer insulation film 130 and the etch stop layer 134, and

providing an electrical connection between the lower electrode 142 of the ferro-electric capacitor and the memory cell transistor; and a second conductor e4 formed to penetrate the first interlayer insulation film 130 and the etch stop layer 134, and providing an electrical connection between the plate transistor and the plate line formed in the second contact hole.

Regarding claims 3-4, Lee also teaches that the etch stop layer 134 is made of SiN material which is etched at a rate slower than a rate at which the first interlayer insulation film 130 of SiO is etched (column 5, lines 1-11). Therefore, it also would have been obvious to form the etch stop layer having etching rate slower than a rate at which the second interlayer insulation film 16 under etch condition used to form the first and second contact holes 17 and 19 for preventing the over-etching to the first interlayer insulation film 11.

Regarding claim 7, as discussed in details above, the combination of Kazushi and Lee substantially reads on the above claim, including the forming of the etch stop insulation layer made of material which is etched at a rate slower than a rate at which the first interlayer insulation film is etched (column 5, lines 1-11). The combination of Kazushi and Lee does not disclose that the etch stop insulation layer is made of a material having an etching rate slower than a rate at which the overlying layer 16 is etched. However, it would have been obvious to form the etch stop insulating layer made of a material having an etching rate slower than a rate at which the overlying layer is etched because as is well known to one of ordinary skill in the art, in order for the etch stop layer functioning as an etch stop, the etch stop layer must have an etching rate

slower than a rate at which the overlying layer is etched for preventing the over-etching to the underlying film or the first interlayer insulation film 11.

Regarding claim 8, Kazushi (Figs. 2 and 8) further discloses: a plate transistor having source/drain regions 4 formed in the semiconductor substrate 1; a second interlayer insulation film 16 formed on the first interlayer insulation film 11 and provided as the overlying layer to cover the ferro-electric capacitor; a first contact hole 17 formed in the second interlayer insulation film 16 to expose the upper electrode 15 of the ferro-electric capacitor; a second contact hole 19 formed in the second interlayer insulation film 16 and located above one of the source and drain regions 4 of the plate transistor; a second contact stud 20 selectively formed in the first interlayer insulation film 11 to make electrical connection to one of the source and drain regions 4 of the plate transistor; and a plate line 18 providing electrical connection between the upper electrode 15 of the capacitor and the second contact stud 20 (see translation, par. [0145]).

Regarding claims 9 and 13, Kazushi further discloses that the overlying layer 16 is a second uppermost level of insulating layer underlying an uppermost level of insulating layer (not shown, see translation, par. [0138]).

Regarding claims 11-12, Kazushi (Fig. 8) further discloses a plate line 18 electrically connecting the contact stud 20 and the upper electrode 15 of the ferro-electric capacitor wherein at least a part of the contact stud 20 contacts the plate line 18 through the contact hole 19 and a portion, surrounding the contact stud of the etch stop

insulating layer 134 (as taught by Lee's Fig. 8) formed under the plate line 18 would contact the plate line 18 through the contact hole 19.

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phat X. Cao whose telephone number is (571) 272-1703. The examiner can normally be reached on Monday - Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PC
May 2, 2005

PHAT X. CAO
PRIMARY EXAMINER